A Fifteen Level Cascaded H-Bridge Multilevel Inverter with Reduced Number of Switches

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Abstract*—Nowadays multilevel inverter (MLI) technologies becomes extremely main choice in the area of high power medium voltage energy control. Although multilevel inverter has a number of advantages it has drawbacks in the layer of higher levels because of using large number of semiconductor switches. This may leads to large size and price of the inverter is very high and also increase in losses. So in order to reduce this difficulties in the new multilevel inverter is proposed to reducing the switches. This paper presents the 15-level cascaded multilevel inverter. The proposed 15-level cascaded multilevel inverter is for reducing the total harmonic distortion which is shown in MATLAB/SIMULINK. The switching pattern of semiconductor switches is used to improve the performance of multilevel inverter. This scheme reduces the switching loss and also increases the efficiency. To authorize the developed technique simulations are carried out through MATLAB/SIMULINK.*

Keywords— Cascaded Multilevel Inverter, Harmonic Distortion, MATLAB, semiconductor switches, THD

I. INTRODUCTION

Multilevel inverters are becoming recent trends, because of its modularity and simplicity of control to generate particular number of levels. Multilevel inverters have a number of applications such as ups, in power grid, as solar inverter, induction heating and number of other applications. By increasing the number of dc voltage sources, a sinusoidal like waveform can be generated. Thus the total harmonic distortions decreases which has a great significance in power grid applications. A sine wave output is desirable because many electrical products are engineered to work best with a sine wave ac power source. The standard electric utility power attempts to provide a power source that is a good approximation of a sine wave.. Switch mode power supply (SMPS) devices, such as personal computers function on quality of sine wave power. Ac motors directly operated on non-sinusoidal power may produce extra heat, may have different speed-torque characteristics, or may produce more audible noise than when running on sinusoidal power thus the multilevel inverters with reduced number of switches becomes more significant. The multilevel inverters is classified as, neutral point clamped inverters, flying capacitor multilevel inverters and cascade multilevel inverters . of this three category cascaded multilevel inverter is recent trend because of its reliability. Table1 shows the comparison of conventional multilevel inverters switching components.

Cascaded multi level inverter uses reduced number of power switches and it produces a sinusoidal like waveform. Cascaded multilevel inverter is series connection of power switches and dc voltage sources. Cascaded multilevel inverters have several advantages when compared to other topologies. The main advantages of using the cascaded multilevel inverters are the high power quality waveforms due to the reduction in the total harmonic distortion and also the reduction of dv/dt stresses on the load, cascaded multilevel inverters can be classified as symmetric and asymmetric multilevel inverters. The main difference between symmetric and asymmetric configuration is the magnitude of dc sources. In symmetric configuration magnitudes of dc sources are same, whereas in the asymmetric configuration magnitudes of the dc sources are different. By using the cascaded multilevel inverters desired number of output voltage levels can be obtained by series connection of a number of dc voltage sources. A number of different topologies have been presented in the literature. Numerous basic units are also presented in the literature. The disadvantage of the symmetric configuration is that it requires more number of power switches when compared to the asymmetric configurations. But the dc voltage magnitude is very high in these papers. Single phase and three phase multilevel inverters can be produced by the series connection of a large number of the basic units.

II. CONVENTIONAL SYSTEMS

The cascaded multilevel inverter to generate output of 5 levels using 8 switches, 7 Levels with 12 switches, 9 levels with 16 switches, and so on. Using 4 switch and one dc source for each h-bridge and produces the one

level of voltage output which is shown in figure1. Common expression for output voltage Levels, $m = (n + 2)/2$ where n is the number of switches in the inverter. Each Bridge is outputting 3 Levels, $+V$dc, 0, $-V$dc.

The number of levels in the three phase circuit means the output phase voltage and line voltage are $2s+1$ and $4s+1$ respectively, where s is the number of H-bridges used per phase. For example, Three H- Bridges, Five H-bridges and Seven H-bridges per phase that is 12 switches ,20 switches, and 28 switches per phase are required for 7-level, 11-level and 15-level multilevel inverter respectively. The value of the ac output phase voltage is the sum of the Voltages produced by each H-bridges.

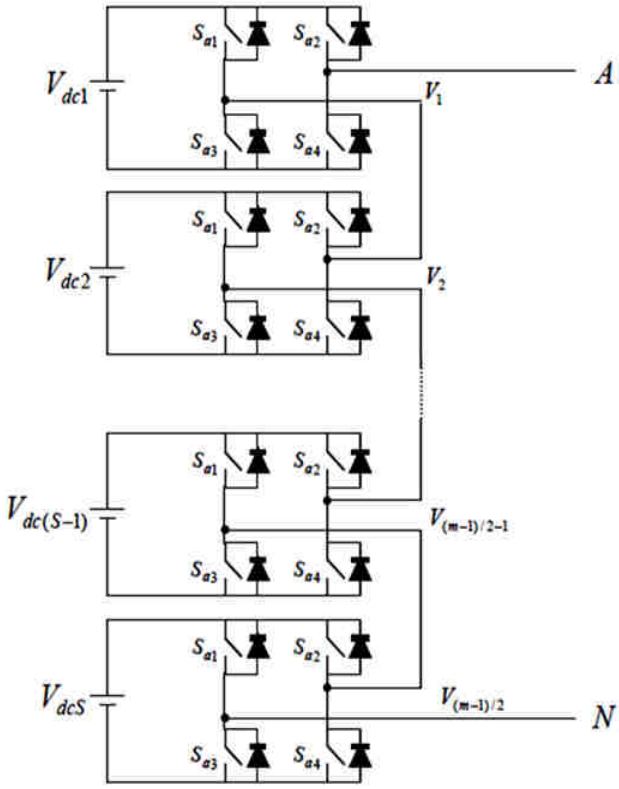


Fig.1. Conventional Cascaded N Level Multilevel Inverter

III. EXISTING SYSTEMS

3.1 7 Level Multilevel Inverter**:**

7-Level, 9 Switche:.This topology which is shown in Figure 2 is built with 3 dc sources, H-bridge composed of 4 switches and then additional 5 more switches which producing the steps of 7 levels, for positive and negative half cycles. Table 2 represent the switching scheme for this topology.

a. 9 Level Multilevel Inverter:

This type of inverter consists of a H Bridge and multi conversion cell which consists of four separate voltage sources (Vdc1, Vdc2, Vdc3 and V dc4), for four switches and four diodes. Each source connected in cascaded with other sources through a circuit consists of one switch and one diode that can create the output voltage source only in positive polarity with a number of levels. Only one H-bridge is attached with multi conversion cell to get both positive and negative polarity.figure3 shows 9 level multilevel inverter and table 3 shows its switching scheme.

First turning on the switch S1 andS2, S3 and S4 will turn off. The output voltage +1Vdc (first level) is produced across the load. Likewise turning on the switches S1, S2 and S3 & S4will turn off to produce voltage +2Vdc (second level) output is produced across the load. Again the process will continue for the voltage level +3Vdc levels can be accomplished by turning on S1, S2, S3 switches (S4 turn off) and +4Vdc levels can be achieved by turning on S1, S2, S3 & S4 as shown in below Table 3

3.3 11 Level Multilevel Inverter:

11 level output voltage we need to connect 5 H-Bridges in cascade., so to attain the higher levels the circuit becomes complex .Three-phase 11 level inverter with less number of power elements and hence less gate drive circuits. Figure 4 shows 11level multilevel inverter and table 4 shows its switching scheme.

3.4 15 Level MLI With 12 Switches:

This asymmetric 15 level multi level inverter topology is made of 12 switches and 3 dc sources and is shown in Figure 5. One H bridge present in the topology is mainly for voltage level change. The switching scheme is given in Table 5.

3.5 15 Level MLI With 10 Switches:

This asymmetric 15 level multi level inverter topology is made of 10 switches and 3 dc sources and is shown in Figure 6. One H bridge present in the topology is mainly for voltage level change. First 6 switches used for level module and H bridge used for voltage shift

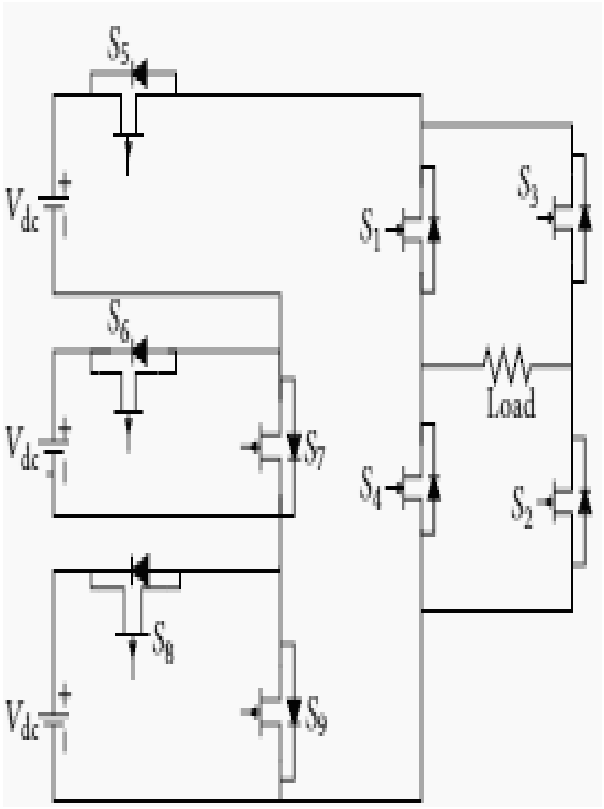


Fig. 2. 7-level 9-switch topology

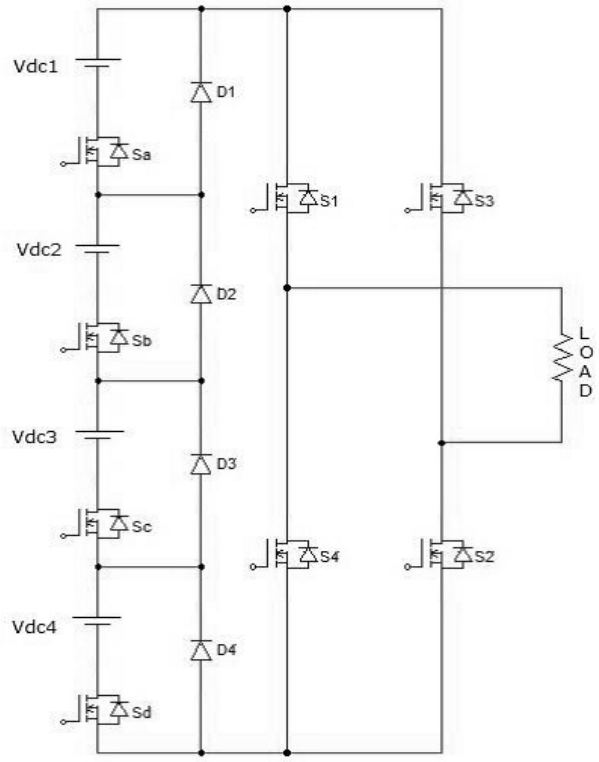


Fig. 3. 9-level cascaded multilevel inverter

Table 2: Switching Scheme for 7-level 9-switch Topology.

Sl.no.	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output voltage	
1	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	+Vdc
2	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	+2Vdc
3	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
5	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	-Vdc
6	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-2Vdc
7	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	-3Vdc

Table 3: switching patterns for 9 levels MC-MLI

S. No	Multi conversion Cell		H-Bridge		Voltage levels
	On switches	Off switches	On switches	Off switches	
1	S1, S2, S3, S4	D1,D2,D3,D4	Q1,Q2	Q3,Q4	+4V_{dc}
2	S1, S2, S3, D4	S4,D1,D2,D3	Q1,Q2	Q3,Q4	+3V_{dc}
3	S1, S2, D3, D4	S3, S4,D1,D2	Q1,Q2	Q3,Q4	+2V_{dc}
4	S1, D2, D3,D4	S2, S3, S4,D1	Q1,Q2	Q3,Q4	+1V_{dc}
5	D1, D2, D3,D4	S1, S2, S3,S4	Q1,Q2	Q3,Q4	0
6	S1, D2, D3,D4	S2, S3, S4,D1	Q3,Q4	Q1,Q2	-1V_{dc}
7	S1, S2, D3,D4	S3, S4,D1,D2	Q3,Q4	Q1,Q2	-2V_{dc}
8	S1, S2, S3, D4	S4,D1,D2,D3	Q3,Q4	Q1,Q2	-3V_{dc}
9	S1, S2, S3, S4	D1,D2,D3,D4	Q3,Q4	Q1,Q2	-4V_{dc}

Table 4: switching patterns for 11 levels MC-MLI

Level Voltages	Switching Pattern							
	S1	S2	S3	S4	S5	S6	S7	S8
+5E	1	0	0	1	1	0	0	1
+4E	0	1	0	1	1	0	0	1
+3E	1	0	0	1	1	0	1	0
+2E	0	1	0	1	1	0	1	0
+E	1	0	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0
-E	0	1	1	0	1	0	1	0
-2E	1	0	1	0	0	1	0	1
-3E	0	1	1	0	0	1	0	1
-4E	1	0	1	0	0	1	1	0
-5E	0	1	1	0	0	1	1	0

Table 5. switching states for fifteen level asymmetric cascaded multilevel inverter

Switching states												Output voltage
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	
1	1	0	0	1	1	0	0	1	1	0	0	7Vdc
0	1	0	1	1	1	0	0	1	1	0	0	6Vdc
1	1	0	0	0	1	0	1	1	1	0	0	5Vdc
0	1	0	1	0	1	0	1	1	1	0	0	4Vdc
1	1	0	0	1	1	0	0	0	1	0	1	3Vdc
0	1	0	1	1	1	0	0	0	1	0	1	2Vdc
0	0	1	1	1	1	0	0	0	1	0	1	Vdc
0	1	0	1	0	1	0	1	0	1	0	1	0Vdc
1	1	0	0	0	0	1	1	0	1	0	1	-Vdc
0	1	0	1	1	1	0	0	0	1	0	1	-2Vdc
0	0	1	1	0	0	1	1	0	1	0	1	-3Vdc
0	1	0	1	0	1	0	1	0	0	1	1	-4Vdc
0	0	1	1	0	1	0	1	0	0	1	1	-5Vdc
0	1	0	1	0	0	1	1	0	0	1	1	-6Vdc
0	0	1	1	0	0	1	1	0	0	1	1	-7Vdc

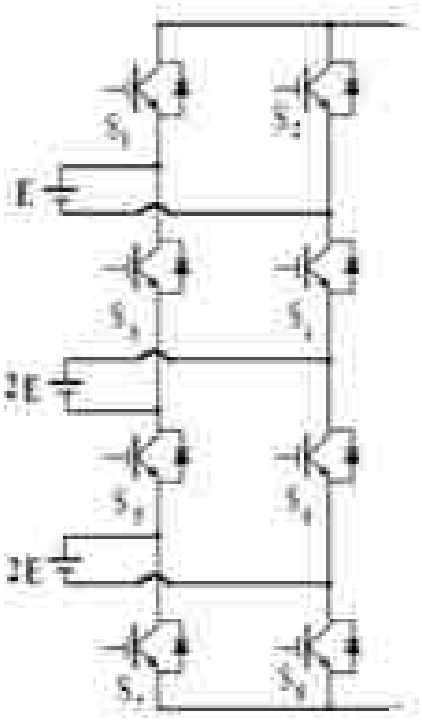


Fig. 4. 11 level multilevel inverter

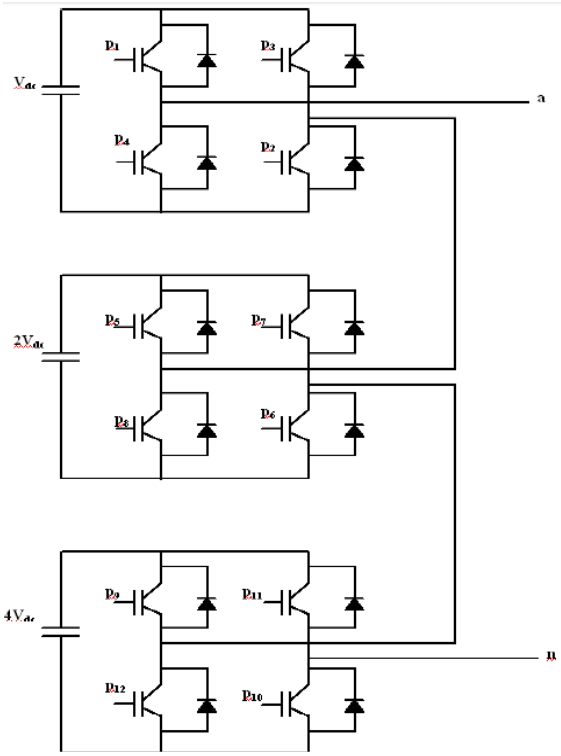


Fig. 5. 15 level MLI with 12 switches

IV. PROPOSED SEVEN SWITCH TOPOLOGY

The projected multilevel inverter has a common structure of the hybrid multilevel inverter is shown in figure7. Every separate voltage source (1vs, 2vs, 4vs) is associated in series by other sources through a unique circuit connected with it. Every step of the circuit consists of only one active switching element and one bypass diode that make the output voltage as positive one with a number of levels. The basic operation of modified hybrid multilevel inverter for getting the output voltage as +1vdc is to turn on the switch s1 (s2 and s3 turn off) and turning on s2 (s1 and s3 turn off) for getting output voltage as +2vdc. Like wise other levels can be accomplished by turning on the appropriate switches at exacting intervals; table7 shows the basic operation of projected hybrid multilevel inverter.

From The Table It Can Be inferred That Only One H-Bridge Is Connected To Get Both Positive And Negative Polarity. Figure7 And Table 7 Shows The Proposed 15 Level Multilevel Inverter Schematic Diagram And Switching Performance.

- The s number of dc sources and the related number output level can be calculated by using the equation n level =2s+1-1
- Voltage on each step can be calculated by using the equation v=2s-1.vdc

- The number of switches used in this topology is given by the equation n switch=s +4

V. SIMULATION CIRCUIT

In The Proposed 15 Level MLI ,The Circuit Is Built Of 7 MOSFET Unidirectional Switches. It Can Also Be Built With 3 Unidirectional 4 Bidirectional Switches. The Load Is Resistive With A Value Of 100 Ohm. Three Asymmetric DC Input Voltages Are Used Having The Values Are 48V, 96V And 192V.Figure8 Shows The Simulation Circuit Of Proposed Topology. Note That In Order To Obtain The Shaped 15-Level Output Without Distortion, MOSFET Block Parameters In MATLAB Should Vary According To The Load. Here For 100 Ohm Resistive Load MOSFET Block Parameters Are Set As Follows:

- FFT Resistance=0.1ohm
- Internal Diode Resistance=0.01ohm

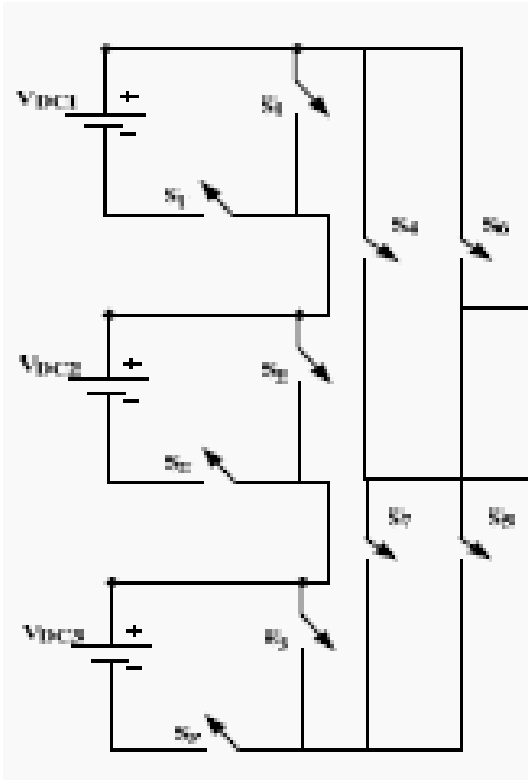


Fig . 6. 15 Level MLI With 10 Switches

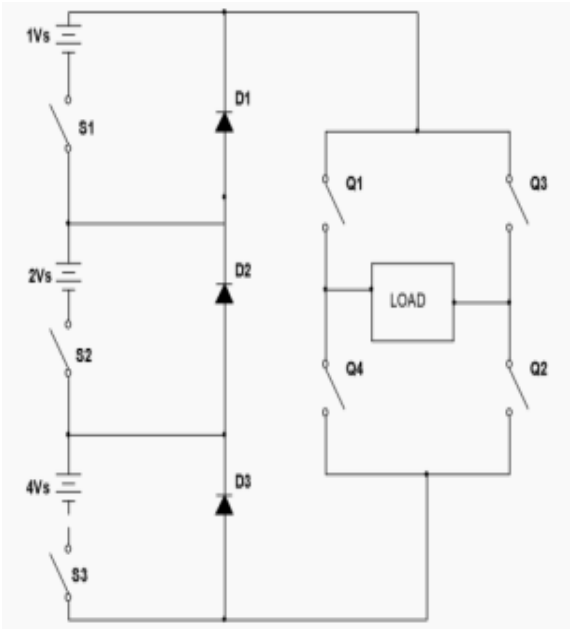


Fig. 7. Proposed Multi level Inverter

Table 6: switching scheme fifteen level asymmetric cascaded multilevel inverter

Sub- Multilevel Switches						H-bridge Switches				Levels
S_1	S_1'	S_2	S_2'	S_3	S_3'	S_4	S_5	S_6	S_7	V_{LI}
0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	1	1	0	0	1
1	0	0	1	1	0	1	1	0	0	2
0	1	0	1	1	0	1	1	0	0	3
1	0	1	0	0	1	1	1	0	0	4
0	1	1	0	0	1	1	1	0	0	5
1	0	0	1	0	1	1	1	0	0	6
0	1	0	1	0	1	1	1	0	0	7
0	1	1	0	1	0	0	0	1	1	8
1	0	0	1	1	0	0	0	1	1	9
0	1	0	1	1	0	0	0	1	1	10
1	0	1	0	0	1	0	0	1	1	11
0	1	1	0	0	1	0	0	1	1	12
1	0	0	1	0	1	0	0	1	1	13
0	1	0	1	0	1	0	0	1	1	14

Table 7: switching scheme of 15 level 7 switch MLI

S.NO	Intervals	On switches	Off switches	Voltage levels	Current flow path
1	I	S1	S2,S3	+1Vs	S1,D2,D3
2	II	S2	S1,S3	+2Vs	S2,D1,D3
3	III	S1,S2	S3	+3Vs	S1,S2,D3
4	IV	S3	S1,S2	+4Vs	D1,D2,D3
5	V	S1,S3	S2	+5Vs	S1,D2,D3
6	VI	S2,S3	S1	+6Vs	D1,S2,S3
7	VII	S1,S2,S3	-	+7Vs	S1,S2,S3
8	VIII	-	S1,S2,S3	0	D1,D2,D3

VI. PULSE GENERATION CIRCUIT

Sine wave voltage is compared with different types of triangular waves to obtain the gate pulses. The relational operators are used. The pulse width of the pulses required determines the value of the constants. Pulse width is determined by the on time of each switch and these signals are used for switching the MOSFETS.

There are four subsystems in this circuit. The comparator compares the triangular and sinewave which gives the required PWM signals. Pulse generation circuit is shown in figure 9.

VII. SIMULATION RESULTS

The waveforms and FFT analysis of 7, 9, 11, 15(12switch), 15(10switch) levels MLI are shown in figure.10, 11, 12, 13, 14. The proposed output voltage and current waveforms and also FFT

analysis are shown in figure 15,16,17. Comparison of FFT analysis with different levels and switches are shown in table 8.

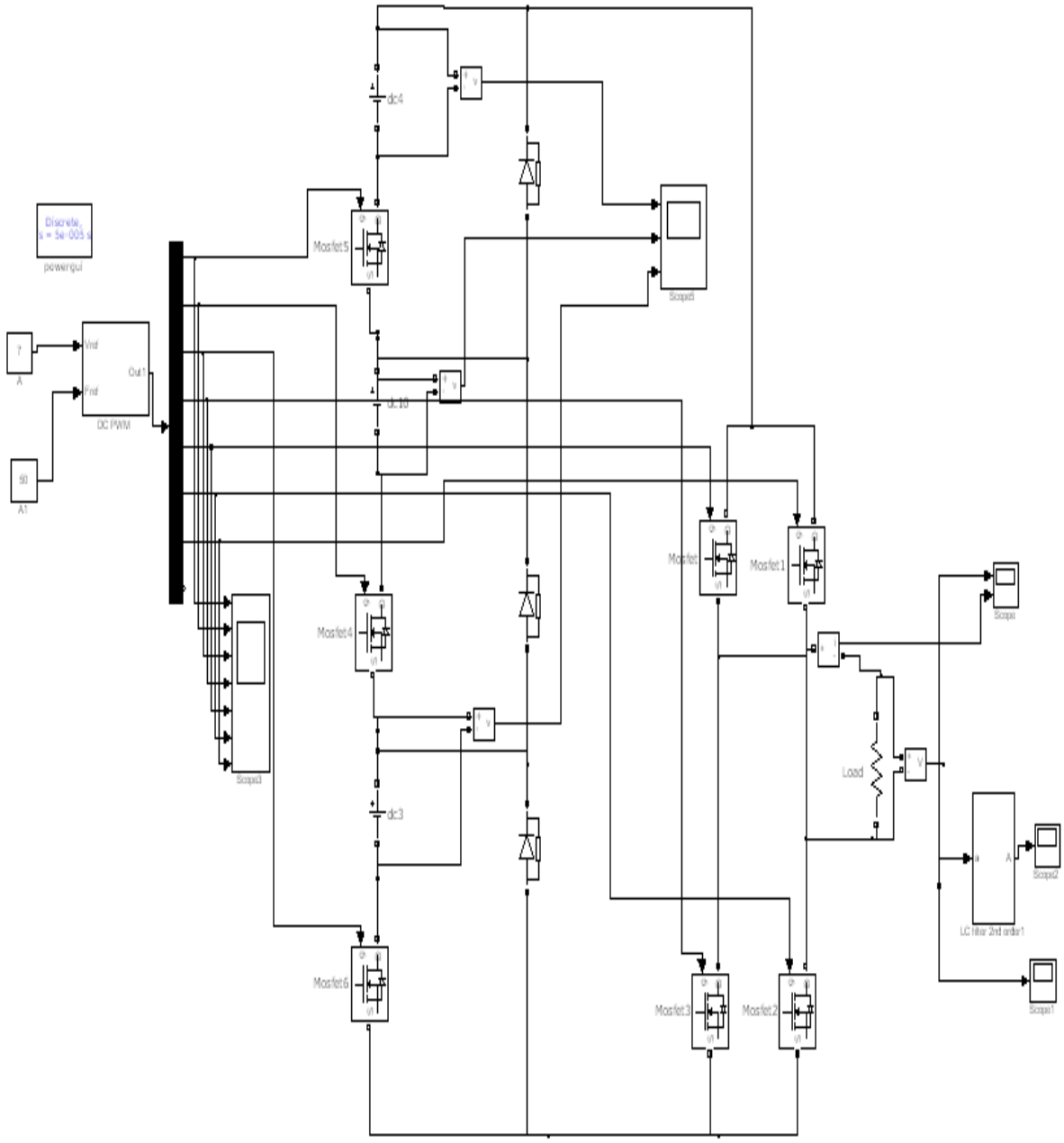


Fig. 8. Simulation Diagram of Proposed Topology

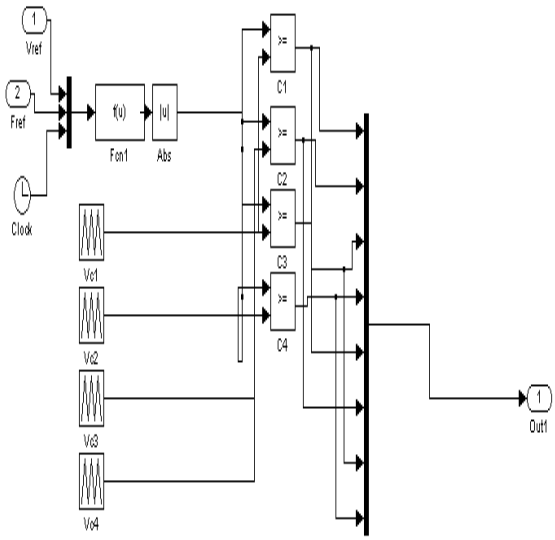
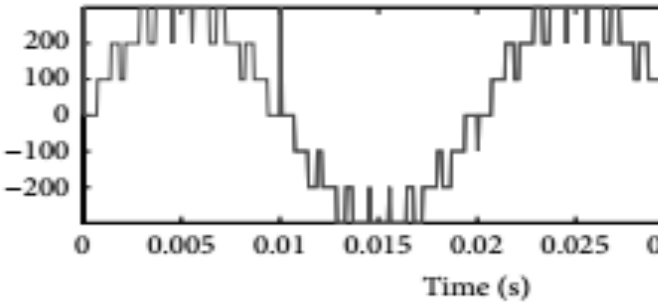


Fig. 9. Pulse Generation Circuit



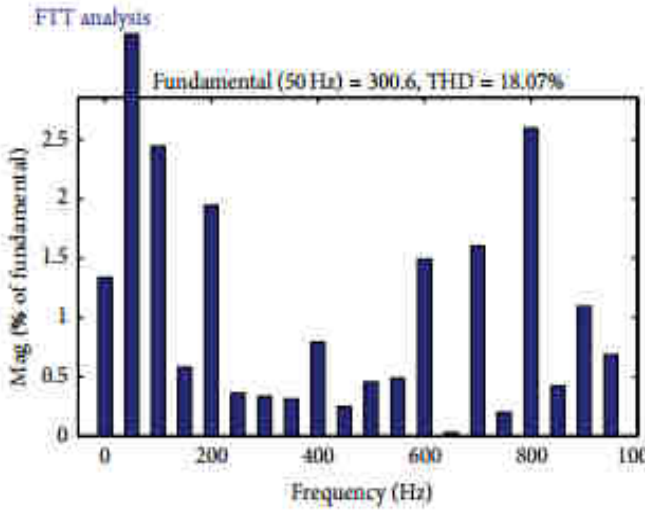


Fig.10 7 level MLI waveform and FFT analysis

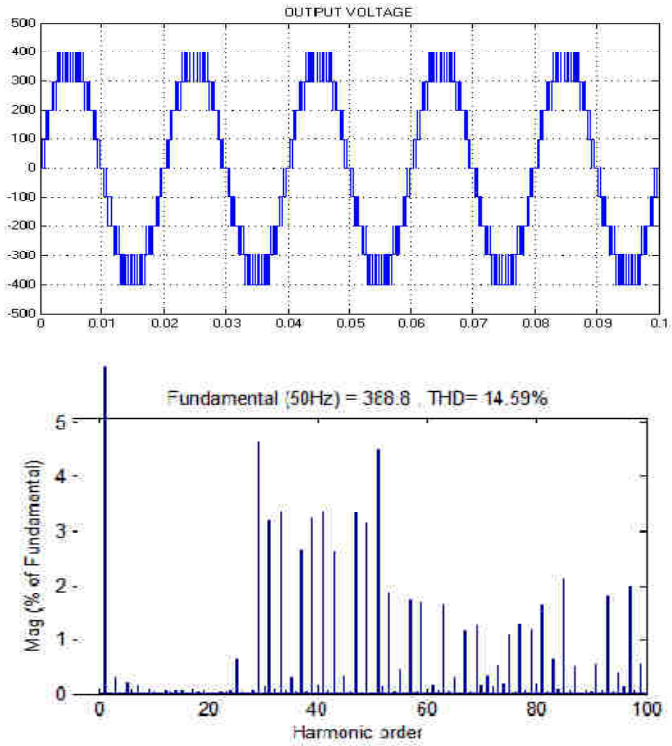


Fig. 11. 9 level MLI waveform and FFT analysis

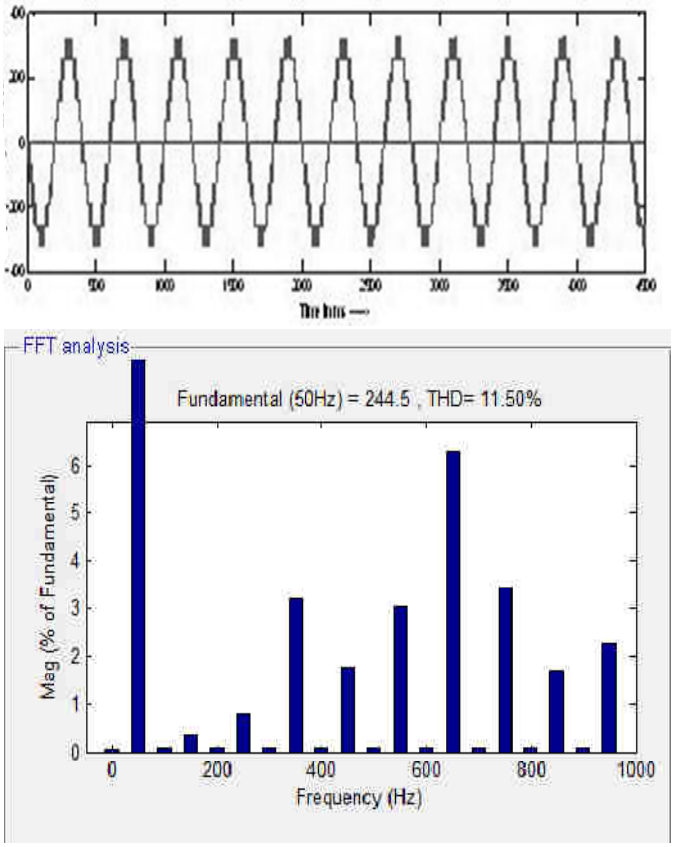


Fig.12. 11 level MLI waveform and FFT analysis

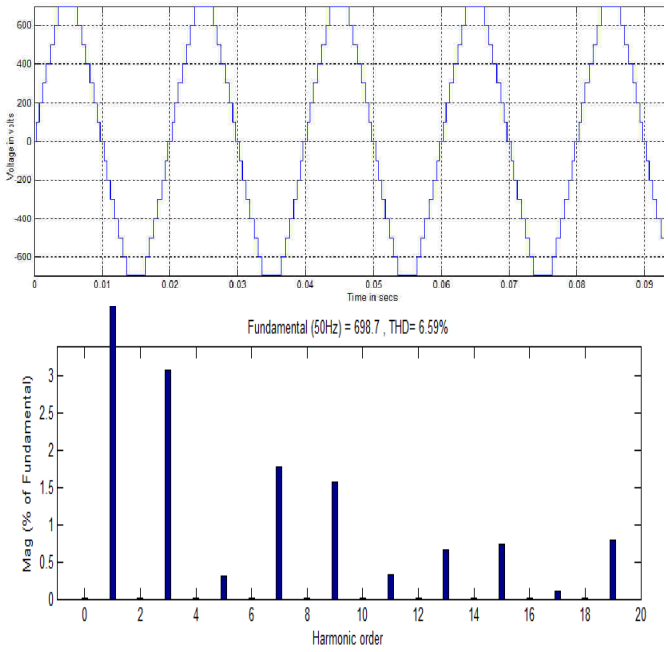


Fig.13.15 level 12 switch MLI waveform and FFT analysis

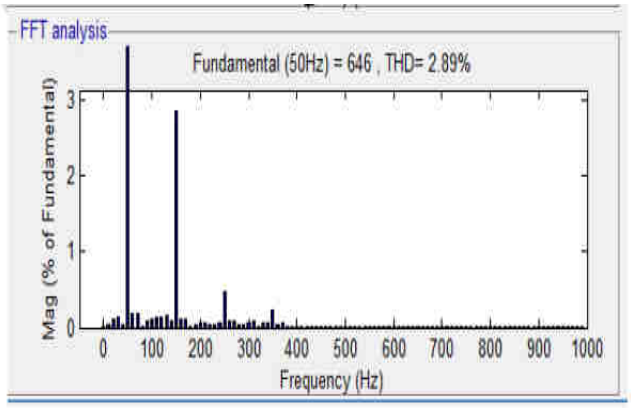


Fig.14.15 level 10 switch MLI waveform and FFT analysis

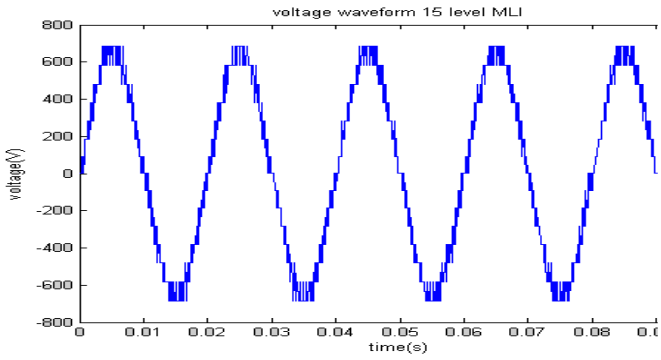


Fig.15. Proposed Output Voltage Waveform

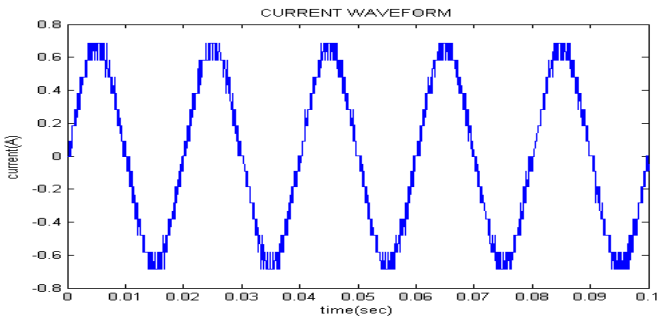


Fig 16.: Proposed Output Current Waveform

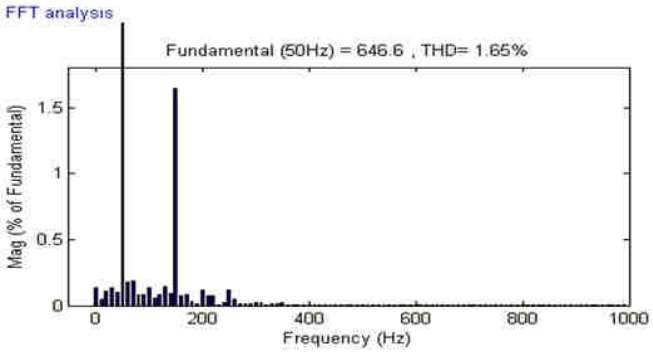


Fig 17: Proposed FFT Analysis Of Proposed System

Table 8: comparison of FFT analysis

Configurations	No. Of Switches	No. Of Dc Sources	THD %
7 level MLI	9	4	18.07
9 level MLI	8	4	14.59
11 level MLI	8	3	11.50
15 level 12 switches	12	3	6.59
15 level 10 switches	10	3	2.89
15 level 7 switches	7	3	1.65

VIII. CONCLUSION

In this projected paper, fifteen level asymmetric cascaded multilevel inverter is presented. The projected inverter can create high quality output voltage close to sinusoidal Waves. It is used to provide improved performance than the conventional cascaded Multilevel inverter. And also this proposed method is used to minimize the switching losses. The total harmonic distortion (THD) can be supplementary reduced.

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